ABSTRACT OF THE DISCLOSURE

A two-wire interface in which upon determining that an operation is to be performed on a slave component, the master component monitors the data wire for a predetermined number of consecutive bits having a particular binary value. Upon detection such a sequence, the master component asserts a frame of a two-wire interface on the data wire. This detected predetermined number of consecutive bits will be considered to be the preamble. During at least some of the preamble phase, the master component is not asserting anything on the data wire. Instead, the data wire is pulled high (or low) by a weak pull-up (or pull-down) resistor. Furthermore, the frame is designed so that there are bits having a guaranteed binary value that is opposite what would be expected in the preamble, to thereby facilitate synchronization.

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